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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/632,550	08/02/2003	Marcos Kamezos	CPAC 1017-7	2570
22470	7590	10/07/2004	EXAMINER	
HAYNES BEFFEL & WOLFELD LLP			TRAN, MAI HUONG C	
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HALF MOON BAY, CA 94019			PAPER NUMBER	

2818

DATE MAILED: 10/07/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

10/632,550

Applicant(s)

KARNEZOS, MARCOS

Examiner

Mai-Huong Tran

Art Unit

2818

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 04 August 2004.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-17 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-17 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 02 August 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

## Attachment(s)

- ☒ Notice of References Cited (PTO-892)
- ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date 1/04, 4/04, 8/04.
- ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- ☐ Notice of Informal Patent Application (PTO-152)
- ☐ Other: \_\_\_\_\_.

## **DETAILED ACTION**

### **Claim Rejections - 35 U.S.C. § 103**

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-4, 7, 10, 11 and 14-17 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Applicant's admitted Prior Art (AAPA) (pages 1-6 and fig. 2) in view of U.S. Patent No. 6,621,169 to Kikuma et al. (hereinafter Kikuma).

Regarding to claim 1, AAPA, in related text ([0019], [0020]), discloses a multi-package module comprising stacked lower and upper packages, each package including a die 24 or 14 attached to a substrate 22 or 12.

AAPA does not disclose the upper and lower substrates are interconnected by wire bonding and at least one package comprises a stacked die package. However, Kikuma teaches the upper 32 and lower substrates 26 that are interconnected by wire bonding 38b (col. 7, lines 3-41, and figure 3), and the package comprises a stacked die package (col. 11, lines 25-67, col. 12, lines 1-5, and figs. 9A, 9B).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the upper and lower substrates that are interconnected by wire bonding, and the package comprises a stacked die package, as taught by Kikuma in order to develop portable electronic devices such as mobile telephones and non-volatile memory media such as IC memory cards have been becoming smaller and smaller. Along with this trend, there have been demands for devices and memory media having a smaller number of components and a smaller size (col. 1, lines 15-20), and without increasing the length of the bonding wires in the packages (col. 5, lines 28-35).

Regarding to claim 2, AAPA discloses the claimed invention except for the lower package comprises a stacked die package. However, Kikuma teaches the package comprises a stacked die package (col. 11, lines 25-67, col. 12, lines 1-5, and figs. 9A, 9B).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the package that comprises a stacked die package, as taught by Kikuma in order to develop portable electronic devices such as mobile telephones and non-volatile memory media such as IC memory cards have been becoming smaller and smaller. Along with this trend, there have been demands for devices and memory media having a smaller number of components and a smaller size (col. 1, lines 15-20), and without increasing the length of the bonding wires in the packages (col. 5, lines 28-35).

Regarding to claim 3, AAPA discloses the claimed invention except for the multi-package module wherein each of the lower package and the upper package comprises a stacked die package. However, Kikuma teaches each of the packages comprises a stacked die package (col. 11, lines 25-67, col. 12, lines 1-5, and figs. 9A, 9B).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form each of the packages comprises a stacked die package, as taught by Kikuma in order to develop portable electronic devices such as mobile telephones and non-volatile memory media such as IC memory cards have been becoming smaller and smaller. Along with this trend, there have been demands for devices and memory media having a smaller number of components and a smaller size (col. 1, lines 15-20), and without increasing the length of the bonding wires in the packages (col. 5, lines 28-35).

Regarding to claim 4, AAPA discloses the claimed invention except for the multi-package module wherein the upper package comprises a stacked die package. However, Kikuma teaches the package comprises a stacked die package (col. 11, lines 25-67, col. 12, lines 1-5, and figs. 9A, 9B).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the package comprises a stacked die package, as taught by Kikuma in order to develop portable electronic devices such as mobile telephones and non-volatile memory media such as IC memory cards have been becoming smaller and

smaller. Along with this trend, there have been demands for devices and memory media having a smaller number of components and a smaller size (col. 1, lines 15-20), and without increasing the length of the bonding wires in the packages (col. 5, lines 28-35).

Regarding to claim 7, AAPA discloses a method for making a multi-package module, providing a stacked die first package, providing a second package, stacking the second package over the first package (fig. 2).

AAPA does not disclose forming electrical interconnects between the first package and the second package by wire bonding. However, Kikuma teaches forming electrical interconnects between the first package and the second package by wire bonding (col. 7, lines 38-41, and figure 3).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form electrical interconnects between the first package and the second package by wire bonding, as taught by Kikuma in order to develop portable electronic devices such as mobile telephones and non-volatile memory media such as IC memory cards have been becoming smaller and smaller. Along with this trend, there have been demands for devices and memory media having a smaller number of components and a smaller size (col. 1, lines 15-20), and without increasing the length of the bonding wires in the packages (col. 5, lines 28-35).

Regarding to claims 10 and 11, AAPA discloses the method of forming a stacked die first package comprises providing an unsingulated strip of stacked die packages wherein a first die 14 affixed to a first package substrate 12, a second die 24 affixed over the first die 14 (fig. 2).

AAPA does not disclose wire bond interconnects between the first and second dies and the substrate. However, Kikuma teaches wire bond interconnects between the first and second dies and the substrate (col. 7, lines 38-41, and figure 3).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form wire bond interconnects between the first and second dies and the substrate, as taught by Kikuma in order to develop portable electronic devices such as mobile telephones and non-volatile memory media such as IC memory cards have been becoming smaller and smaller. Along with this trend, there have been demands for devices and memory media having a smaller number of components and a smaller size (col. 1, lines 15-20), and without increasing the length of the bonding wires in the packages (col. 5, lines 28-35).

Regarding to claim 14, AAPA discloses the method further comprising attaching second-level interconnect balls onto the first package substrate (fig. 2).

Regarding to claim 15, AAPA discloses the method further comprising encapsulating the stacked packages on the module in a molding compound 27 (specification: [0019], fig. 2).

Regarding to claim 16, AAPA discloses a mobile device comprising the multi-package module (specification: [0004]).

Regarding to claim 17, AAPA discloses a computer comprising the multi-package module (specification: [0004]).

Claims 5 and 12 are rejected under 35 U.S.C. 103 (a) as being unpatentable over AAPA in view of U.S. Patent No. 6,621,169 to Kikuma et al. and further in view of LoBianco et al. (US 6,340,846) (hereinafter LoBianco).

Regarding to these claims, AAPA in view of Kikuma discloses the claimed invention except for the adjacent stacked dies in the stacked die package are separated by a spacer. However, LoBianco teaches the adjacent stacked dies in the stacked die package are separated by a spacer 50 (col. 6, lines 49-52, and fig. 8).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the adjacent stacked dies in the stacked die package that are separated by a spacer, as taught by LoBianco in order to enhance component density of the package and to provide a simple, inexpensive method for making a semiconductor



package with stacked dies that eliminates fracturing of the dies during the wire bonding process or as a result of incompatible thermal expansions, and that also eliminates the problem of broken wire bonds as a result of wire sweep (col. 1, lines 38, lines 54-59).

Claims 6 and 13 are rejected under 35 U.S.C. 103 (a) as being unpatentable over AAPA in view of U.S. Patent No. 6,621,169 to Kikuma et al. and further in view of Bertin et al. (US 5,977,640) (hereinafter Bertin).

Regarding to these claims, AAPA in view of Kikuma discloses the claimed invention except for the multi-package module further comprising a heat spreader over the second package. However, Bertin teaches the heat spreader over the component (col. 4, lines 16-17, and fig. 7).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the heat spreader over the component, as taught by Bertin in order to allow for heat dissipation for chip-on-chip component (col. 4, lines 18-19).

Claims 8 and 9 are rejected under 35 U.S.C. 103 (a) as being unpatentable over AAPA in view of U.S. Patent No. 6,621,169 to Kikuma et al. and further in view Akiba et al. (US Pub. No. 2004/0016939) (hereinafter Akiba).

Regarding to claim 8, AAPA in view of Kikuma discloses the claimed invention except for the method wherein providing a stacked die first package comprises testing

stacked die packages for a performance and reliability requirement, and identifying a package that meets the requirement as a first package. However, Akiba teaches testing packages (page 8, [0078]).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to test packages, as taught by Akiba in order to improve manufacturing yields and reduce costs (page 8, [0074]).

Regarding to claim 9, AAPA in view of Kikuma discloses the claimed invention except for the method wherein providing a second package comprises testing packages for a performance and reliability requirement, and identifying a package that meets the requirement as a second package. However, Akiba teaches testing packages (page 8, [0078]).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to test packages, as taught by Akiba in order to improve manufacturing yields and reduce costs (page 8, [0074]).

### Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mai-Huong Tran whose telephone number is (571)272-1796. The examiner can normally be reached on 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571)272-1787. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

*mh*  
10/4/04

  
Mai-Huong Tran  
Examiner  
Art Unit 2818